Chip Scale Package Fiber Optic Transceiver Integration for Harsh Environments

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Abstract: We present fiber optic technology for 850 nm, VCSEL-based embedded optical computing solutions. We introduce concepts for compact, rugged fiber optic transceivers that provide multi-channel operation at 12.5 Gbps per channel. The transceiver can be placed in close proximity to high performance ASICs to provide direct optical I/O between components. The transceiver is packaged with material having material having match coefficients of thermal expansion (CTE), and expanded beam optical interface – these features offer survivability and operation over wide temperature ranges.

Keywords: VCSEL, chip-to-chip optical interconnect

Introduction

There is considerable interest in the commercial markets to reduce the power consumption associated with data communications over copper interconnect. The availability of high performance ASICs, such as FPGAs, that have 10’s of channels operating at data rates above 10 Gbps have created a trend to place optical transceivers near the ASIC. The objective is to minimize the signal loss and power consumption associated with driving high speed signals across copper traces. The traditional PCB layout places the optical transceivers near the edge of the PCB, far away from the centrally located ASICs. In this situation, a more than 50% of power consumed in both the ASIC and transceiver is dedicated to driving high speed signals across the PCB. Optical interconnect also allows an increase in channel density without the EMI related crosstalk penalties.

This solution requires a unique packaging approach, as compared to traditional fiber optic modules. Several companies are developing advanced packaging to make embedded optical modules (EOM) possible [1-4]. These efforts created compact 1 x 12 transmitter and receiver components (called microPODs™), with each channel operating at 10 Gbps.

However, the EOM components may be placed in such close proximity to the ASIC that the local temperature is much higher than the typical 70 C rating of fiber optic transceivers. High performance computing ASICs can draw ~100 W of power, raising the operating temperature for nearby components. There is also a trend for data centers to operate equipment at a higher temperature to reduce the costs of cooling. A transceiver that can operate reliably at higher temperature (~100 C) is needed for these applications.

Chip-Scale-Packaged Embedded Optical Modules

To operate at high temperatures, the EOM must be constructed of materials that can withstand high temperature (ideally compatible with solder reflow) and maintain efficient optical coupling over wide temperatures. The CORE is an ‘optical engine’ that performs the electrical to optical signal conversion. The CORE has an electrical wire-bond interface to the PCB. The CORE (see Figure 1) contains the transceiver ASIC, VCSEL (4x) and PIN (4x) arrays, collimating optics and mechanical features for alignment to a fiber connector. The CORE footprint is 8 x 8 mm² and the height is 1.2 mm. The VCSEL has an efficient thermal path to the bottom of the CORE (with a measured ΔT < 8° between VCSEL and package case in the configuration described in this white paper).

Figure 1: The. CORE. is. a. flip.chip. assembled. optoelectronic. component.with.integrated.coupling.optics..

The cross-section of the CORE in a FR-4 arrangement with a ruggedized vertical connector (RVCON™) is shown in Error! Reference source not found. The CORE to RVCON™ optical interface uses collimated beams (aka, expanded beam interface, but at a micro-scale). This interface relaxes the alignment tolerance at the connector interface. This interface uses four ‘expansion joints’ to accommodate the CTE mis-match between the RVCON™ and CORE materials. This interface has been verified over thermal cycling between -55 C to 125 C to be mechanically

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sound, with less than 1 dB loss and 1 dB variation in optical coupling.

**Next Generation EOM with Chip Scale Packaging**

Next generation EOMs can bypass the semiconductor package and create transceivers based on chip scale packaging (CSP). The CORE as a stand-alone transceiver, eliminates extraneous parts, and offer electrical I/O paths that will support bandwidths of 25 Gbps. The concept is shown in figure 2.

![Figure 2 CSP Transceiver Design.](image)

The component is assembled on a transparent carrier, which can either be sapphire or glass. We currently use sapphire (as our existing component has some support circuitry – thus, we use silicon-on-sapphire circuitry), but we plan to migrate to glass to reduce costs. The transceiver ASIC, OE devices and electrical I/O are on the bottom side of the carrier. A lens component is aligned and attached to the top of the carrier. This component is a stack containing collimated optical lenses, which are sealed, and a silicon layer. The silicon layer has mechanical features for attachment of a fiber connector and openings to allow the light to pass.

In this configuration, the transparent carrier has electrical signal routing that interconnects the ASICs, OE chips and copper-posts. The carrier is created in a wafer process that creates copper posts (sometimes called ‘pillars’) topped with solder caps. This process has been developed to support flip-chip ASIC packaging and is a variant of IBM’s C4 process (controlled collapse chip connection).

The carrier size is 7.7 mm x 8.3 mm with 80 electrical I/O. While the current layout is for a 4+4 format, we reserved the area for the additional I/O needed for a 1 x 12 format (either a 1 x 12 transmitter or 1 x 12 receivers). Therefore, the carrier will support either 4 + 4 or 1 x 12 formats with a simple change to the routing metallization on the carrier.

The electrical connections on the carrier should support high speed routing. The copper-post spacing and routing were designed to match 50 ohms. We modeled the electrical crosstalk between channels and found better than 30 dB of isolation.

Early integration of this CSP approach is shown in Figure 3 below.

![Figure 3 - CSP Transceiver 4x4mm](image)

**Conclusion**

We present methods of creating compact fiber optic transceivers for that can operate over wide temperatures. This approach has promise to significantly reduce the cost of transceiver components and assembly processes, bringing the cost in-line with that of current commercial transceivers. The approach enables the incorporation of advanced built-in-test and solderable transceiver components.

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