14/16nm FinFET Radiation Response Characterization

Jeffrey Kauppila¹, Hui Jiang¹, Hangfang Zhang¹, Thiago Assis¹, T. Daniel Loveless², Tim Haefner¹, Andrew Sternberg¹, Dennis Ball¹, Jason Rowe¹, Bharat Bhuva¹, Michael Alles¹, Lloyd Massengill³

¹Department of Electrical Engineering and Computer Science
Vanderbilt University
Nashville, TN, USA

²Electrical Engineering Department
University of Tennessee at Chattanooga
Chattanooga, TN, USA

Abstract: Radiation response characterization test chips have been designed and fabricated for bulk and SOI FinFETs at the 14/16nm technology node. Heavy-ion data, over ion energy and supply voltage, shows bulk FinFET NAND-based DICE-style flip-flop designs to be significantly harder than standard D-Flip-Flop (DFF) designs for normal incidence irradiation. Heavy-ion irradiation data for the SOI designs will be included in the conference presentation and paper.

Keywords: Single-event upset, FinFET, bulk, SOI, DICE, flip-flop

Introduction
Single-event upset and single-event transients are an increasing concern in highly-scaled CMOS technologies [1]. The scaling of CMOS to the sub-20nm node has introduced the disruptive 3D FinFET geometry to an already complex radiation hardened design space. This work presents results from radiation testing on technology and circuit characterization test chips fabricated in 16nm bulk FinFET and 14nm SOI FinFET technologies. Normal incidence heavy-ion tests have shown DICE designs to have a single-event upset (SEU) cross sections of one to three orders of magnitude less than those observed in standard DFF designs.

Overview of Test Chips
Two radiation characterization test chips have been developed to experimentally evaluate the radiation-induced response of circuits built in FinFET technologies. One test chip, comprised primarily of CREST style flip-flop shift registers, was built in a commercially available 16nm bulk FinFET technology [2]. The test chip floor plan, highlighting the location of the CREST style circuits, is shown in Fig. 1. Another test chip, containing two flip-flop shift registers, a single-event transient (SET) measurement circuit, ring oscillators, arrays of transistors, and an RF NMOSFET device, was designed and fabricated in a 14nm SOI FinFET technology. The test chip utilized C4 pad-array I/O for the circuit macros, which will be bonded via flip-chip techniques on a custom interposer, and probe pads for the transistor arrays and the RF NMOSFET characterization. Fig. 2 shows a die photograph of the SOI FinFET test chip, where the C4 solder balls and the probe pads are clearly visible.

The bulk FinFET test chip was designed in collaboration with the Soft Error Consortium, which is comprised of industry and university groups. In this work, we will present data from the university designs. The baseline unhardened design is a clocked-inverter-based DFF, and
the hardened designs include NAND-based DICE-style flip-flops [3]. The test chip contained three spacing variants of the DICE design, where the sensitive node pairs were spaced by 0.65 μm, 1.19 μm, and 1.73 μm for the compact, medium, and spread designs, respectively. The data presented here is for the medium spaced design, however all three designs exhibited qualitatively similar responses. A schematic representation of the NAND-based DICE design is shown in Fig. 3.

The SOI FinFET test chip contained a DFF shift register using a standard transmission-gate-based design and shift register utilizing transistor stacking as a hardening method [4], [5]. The SET measurement circuit utilized a long chain of inverters as the target for SET generation and four delay based measurement circuits with no-delay, a 2-inverter delay, a 4-inverter delay, and an 8-inverter delay. The number of delay-based circuits that toggle provide a bound for the pulse width, in terms of inverter delay.

Radiation Experiments

The 16nm bulk FinFET test chips were heavy-ion irradiated in June and December 2015 at Lawrence Berkeley National Lab (LBNL) using the 10 MeV/amu and 16 MeV/amu cocktails [6]. The test results presented here are for normal incidence. The ions used in the experiment are provided in Table 1. The 16nm bulk FinFET test chips have also been irradiated using a 10 μCi Americium-241 isotropic button source that emits alphas at a rate of approximately 1000 alpha/mm²/s with a mean energy of approximately 5.4 MeV. Isotropic alpha irradiation and Pelletron ion-beam data from experiments performed at Vanderbilt University on the 14nm SOI test chip will be included in the conference presentation.

The parts were tested over multiple core-supply voltages, from the nominal 0.8 V down to 0.55 V, to assess the impact of voltage scaling on the SEU sensitivity of the circuits. The parts were also tested over frequency, from 50kHz to 1.3GHz, to assess the impact frequency on the susceptibility to single-event upset.

Radiation Test Results

The SEU cross-sections are calculated as

$$\sigma = \frac{n_{SEU}}{F \times N_{FF}}$$

where \(n_{SEU}\) is the number of measured single-event upsets, \(F\) is the total fluence of particles/cm², and \(N_{FF}\) is the number of flip-flops in the CREST block shift register. The error bars are calculated as the standard error of measurement (StdErr)

$$StdErr = \sqrt{\frac{n_{SEU}}{F \times N_{FF}}}$$

In the cases where no upsets were measured, the SEU cross section is recorded as less than the limiting cross section. The limiting cross section is traditionally calculated as

$$\frac{1}{F \times N_{FF}}$$

The heavy-ion test data shows that the saturated SEU cross sections for the unhardened 16nm bulk FinFET flip-flops are comparable to the saturated SEU cross sections from similar flip-flop designs in the bulk 28nm and 20nm planar technologies, however the threshold LET and low-LET cross sections show improvement over the previous bulk technology nodes. At the highest tested LET values, the 16nm DICE designs are at least three orders of magnitude harder than the unhardened clocked-inverter based D-flip-flop design. Fig. 4 shows the SEU cross-section trend for an unhardened flip-flop design in 28nm bulk planar CMOS to 16nm bulk FinFET technologies [8]. For comparison, Fig. 4 also includes a similar flip-flop design from a 32nm partially depleted SOI technology [9].

Isotropic alpha and heavy-ion testing performed over VDD, from 800 mV to 550 mV, showed a strong bias dependence on the SEU cross sections for unhardened and DICE flip-flops. Fig. 5 shows the SER (all 0 input) for four unhardened, clock-inverter flip-flop designs, where the only variation between designs was the selection of transistor threshold voltage. Fig. 5 shows the largest SER was measured for the flip-flop utilizing the transistors with the highest threshold voltage (SVT), and the smallest SEU cross section was measured for the flip-flop utilizing transistors with the lowest threshold voltage (ULVT). The scaling trend observed in Fig. 4, can also be observed in Fig. 6, where the SER from reduced VDD supply isotopic alpha testing in identical topology 20nm planar bulk CMOS and 16nm bulk FinFET flip-flops are shown. The

![Figure 3. Schematic of DICE latch and flip-flop design](image-url)
20nm flip-flop in Fig. 6 was not functional below a VDD voltage of 800 mV.

Fig. 7 shows the heavy-ion test results for the highest threshold voltage unhardened flip-flop variant (SVT) from Fig. 5, where the VDD supply was varied from 800 mV to 550 mV. The reduced VDD supply voltage resulted in a 3X increase in the measured SEU cross section. Figs. 8 and 9 show the heavy-ion test results for two of the three DICE variants, the 0.65μm sensitive node spacing and 1.73μm sensitive node spacing, respectively. There were no upsets observed at the nominal supply voltage, however multiple upsets were recorded for some LET values at reduced supply voltages. The smallest sensitive node spaced DICE design had more upsets than the largest sensitive node spaced DICE design at reduced bias, which highlights the impact of charge sharing required to upset the cell.

Fig. 10 shows the results of heavy-ion testing over operating frequency at nominal VDD for the DICE sensitive node spacing variants. The DICE shift register utilized a Q to D connection resulting in a susceptibility to single-event transients generating upsets while propagating between the master and slave stages in the flip-flops or between flip-flops [10]. Fig. 10 shows an increasing SEU cross-section for increasing clock frequency from 400 MHz to 1.3 GHz. In all cases, the measured SEU cross-section for increased frequency is above the limiting cross section of 2.4x10^{-12} cm^2/FF.

Conclusions

Two test chips have been designed in bulk and SOI FinFET process to assess the radiation response of circuits built in FinFET technologies. The 16nm DFF and DICE data suggests and DICE latches remain significantly harder than DFF designs for normal-incidence irradiation. Future tests of the SOI test chip and angled testing of the bulk test chip will further clarify the radiation response characteristics of these circuits and elucidate mechanisms for modeling radiation effects in FinFET technologies, with the goal of providing radiation-enabled models to the radiation-hardened circuit design community. Additional data from test chips will be presented in the conference presentation.
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References


