Abstract: DoD has need for small quantities of custom Trusted advanced Rad-Hard microchips. But the cost of masks used in optical lithography has soared and continues to rise unabated. Multibeam has developed maskless electron-beam lithography (EBL) for producing advanced Rad-Hard and other DoD microchips at lower cost. In addition to significant cost savings in mask and lithography equipment, Multibeam’s maskless EBL technology is capable of providing other benefits including enhanced security of individual ICs and the supply chain, extending lithography capability to more advanced technology nodes, and reduced cycle time and cost in prototyping new ICs. This paper examines Multibeam’s maskless lithography approach and reviews the programs supported by AFRL, DTRA, and SMC to develop production systems for Trusted Foundries.

Keywords: Rad hard microchips (RHIC); maskless electron-beam lithography (EBL); e-beam direct write (EBDW); complementary e-beam lithography (CEBL); multiple patterning; cycle time; counterfeiting; anti-tamper.

Introduction

The DoD has a critical, on-going need for custom high-performance, low-power, radiation-hardened microchips produced at secure facilities in small quantities, over extended program lifetimes. These microchips are crucial in enabling satellite, intelligence, battle systems and warfighter capabilities. But the Trusted Foundries that produce the microchips used in our National Defense are facing serious challenges.

To meet the performance and power requirements of current and future DoD Programs, Trusted and Qualified production facilities need to provide a continuous guaranteed source of increasingly advanced microchips. However, each new chip technology generation demands ever-larger capital outlays for lithography equipment and higher operating expenses due to photomask (mask) cost.

Moreover, optical lithography equipment is designed for high-volume manufacturing and unsuited for production of small quantities of a wide mix of special devices for DoD. The Defense Science Board Task Force on High Performance Microchip Supply recommends, “New methods and equipment concepts must be found that make custom circuit fabrication economical.”[1]

Multibeam Maskless EBL for DoD IC Production

Multibeam Corporation (Multibeam, Santa Clara, CA) has developed innovative technology in maskless electron-beam lithography (EBL), also known as e-beam direct write (EBDW). Multibeam’s EBL is well suited for producing advanced Rad-Hard ICs with high performance, high reliability, and low-power. Multibeam’s EBL also significantly improves anti-counterfeiting and supply chain traceability to meet DoD and OGA demands for anti-tamper and Trusted microelectronics, including ROICs, FPGAs, and Classified ICs. DTRA, NRO, SMC, AFRL, Aerospace, and Sandia have identified the ongoing need. This is summarized in Table 1.

Multibeam completed extensive simulation and analysis of low-energy (5 keV) maskless EBL. The study showed that similar to optical lithography, low-energy maskless EBL has no negative effect on RHICs.

Multibeam is completing feasibility demonstrations of major subsystems for multi-column maskless EBL in Q1 2016 and is on plan to start the next phase in building a maskless EBL production system for Trusted fabs.

Table 1. Multibeam Maskless EB Lithography Supports DoD/OGA Needs

<table>
<thead>
<tr>
<th>Trusted Supply Chain</th>
<th>Space/Nuclear</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Anti-counterfeit ICs</td>
<td>• Rad-hard compatible</td>
<td>• Less litho capital expenditure</td>
</tr>
<tr>
<td>• ICs with unique IDs</td>
<td>• High reliability</td>
<td>• Cut mask cost (&lt; $20M/year)</td>
</tr>
<tr>
<td>• Secure encryption keys</td>
<td>• Large-format ROICs</td>
<td>• Reduce IC re-design cost</td>
</tr>
</tbody>
</table>
Semiconductor Lithography Development Update

Recapped below are key developments leading to today’s high cost in semiconductor lithography.

Around 2004 when 90nm ICs went into volume production, the cost of masks had already surged. Mask cost has since escalated unabated, Table 2.

Table 2. Mask cost increases since 90nm node

<table>
<thead>
<tr>
<th>Technology node</th>
<th>90nm</th>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$ Million per mask Set</td>
<td>1.0</td>
<td>2.5</td>
<td>3.5-4</td>
<td>5</td>
</tr>
</tbody>
</table>

Since 2007 when 193nm immersion (193i) – the state-of-the-art optical lithography – reached its 80nm resolution limit, there has been no resolution improvement in optical lithography equipment.

To enable manufacture of advanced designs, Intel was first to adopt unidirectional (1D) layout with “lines and cuts” to replace conventional random 2D layout. [2] Today, 1D layout style is employed throughout the industry at ≤ 28nm.

The 1D layout in GDS file decomposes into “line” and “cut” patterns, enabling 193i to print both lines and cuts. While 193i can print uniform lines very well, printing cuts turns out to be increasingly costly for each advancing node.

193i printing cut patterns now requires “multi-patterning”. In multi-patterning, a cut layer is split into multiple layers, each of which contains cut features that are separated more than 80nm – the limit of 193i resolution. And the wafer must pass through the 193i equipment 2, 3, or 4 times (i.e., double, triple, or quadruple patterning) to pattern one layer.

The layers needing 193i multi-patterning are called “critical layers” as they are most challenging and costly to pattern. These layers include line-cuts in gate and metal layers as well as holes in contact and via layers.

The number of critical layers grows as technology nodes get smaller. For example, at 14nm node, there are at least 13 critical layers; at 10nm node, the number increases to 26 or more.

193i multi-patterning is the direct consequence of the 193i resolution limit. The negative effects have now spread from increased mask/equipment costs to increased mask steps to squeezed error budget for each critical layer to product yield and cycle time. Unfortunately, 193i is the industry’s default lithography solution.

What Exactly is CEBL?

It’s well known that e-beam lithography needs no masks and affords high resolution, and is an essential tool in the R&D lab. However, its low throughput has historically kept it out of any production environments even if low volume.

Multibeam’s maskless EBL is a new breed of EBL. It’s designed to pattern cuts and holes in critical layers to replace 193i multi-patterning and complement 193i. EBL for complementary use is known as complementary EB lithography or CEBL [3-4] – a relatively new industry acronym.

Figure 1 shows how Multibeam’s CEBL and 193i work in tandem: 193i prints “lines”, doing what it does best, then e-beam writes “cuts” (of the lines) directly on wafer without masks. CEBL also patterns contact and via holes.

How Is CEBL different from other EB systems?

CEBL is far different from other e-beam maskless lithography called ML or ML2.

ML systems are designed to pattern random 2D layouts for any and all layers on wafer, replacing 193i as the next generation lithography (NGL). Typically, ML systems employ a single e-beam column, writing pixel by pixel, scanning the whole wafer. Empirical data collected over some 30 years and published in 1999 show that such EBL systems suffer from rapid deterioration in throughput as resolution improves. Even if the single e-beam is split into hundreds of thousands of beamlets, ML systems are too slow for wafer production. [5]

As a dedicated complementary tool, Multibeam’s CEBL is not NGL seeking to supplant 193i. Our CEBL deployment requires no new infrastructure. In fact, it helps extend the productive use of optical lithography. [6]
To overcome e-beam’s inherent limitation in throughput, Multibeam takes a fresh approach to maskless CEBL:

- Columns are made very small, so multiple-columns can be deployed in a modular array. Multi-column parallel writing is faster than single-column writing used in the past.
- Each column writes shots with a shaped beam. Each shot patterns one cut or hole in a critical layer. Writing each cut with one shot, rather than writing hundreds of pixels, reduces write time as well as system complexity.
- The beam is vector-scanned to skip 95% of the wafer where there are no cuts, dramatically boosting speed.

A single-module CEBL system writes 5 wafers per hour, which is good for low-volume production and prototyping.

What Are CEBL’s Benefits to DoD?

Multibeam’s CEBL provides major benefits to DoD: CEBL lowers IC production cost, reduces prototyping cost & time, eliminates mask-related security risks, enhances IC security, extends to future technology nodes, and provides process flexibility. These benefits are highlighted below:

Reduce mask/equipment costs for production:

In high volume manufacturing, lithography now accounts for more than 50% of wafer cost. In low volume production, lithography may account for an even greater portion of wafer cost.

Mask cost: As shown in Table 2, previous page, mask cost jumps with each technology node at ≤ 90nm due to increased mask complexity and number of masks in a set. CEBL patterns directly on wafer with no masks.

Lithography equipment cost: 193i equipment is designed for high volume manufacturing and is priced accordingly at $90M each. Multibeam ensures the availability of low-volume lithography to Trusted fabs at much lower cost.

Cut prototyping cost and cycle time:

CEBL helps reduce prototyping cost in developing new or derivative microchips. This is because design changes in IC development can be implemented directly in the CEBL Cut database at the Trusted Foundry, with no need for new masks. By eliminating masks, re-spin cycle time is reduced from weeks to hours, enabling faster time-to-deployment.

Eliminate mask-related security vulnerability:

To make an optical mask, a process known as “data prep” is applied in which the GDS design file is accessed and changes are made to the design data. The changes involve optical proximity corrections and other resolution enhancements, plus adding dummy features to improve etch and CMP processes. At advanced technology nodes, the resulting layout data volume and complexity make it virtually impossible to verify trustworthiness.

The Defense Science Board Task Force on High Performance Microchip Supply noted this security vulnerability, “The activities in [mask data prep] are those that entail direct access to the chip design database and are thus very high risk.” [1]

In 1D “Lines and Cuts” layout, the critical design data reside in the CEBL cut database. The “line mask” is made up of uniform lines and contains no critical information. The security advantage of maskless EBL is compared to current practice in Figure 2, below.

Figure 2. Critical design data protected with secure database transfer directly to Trusted Foundry.
DoD Support and Production System Roadmap

With support from DTRA, AFRL, and SMC, Multibeam has made steady progress toward developing a maskless EBL production system. Multibeam’s roadmap is illustrated in Figure 3, above.

DTRA was first to support this multi-year maskless EBL effort. The DTRA project focused on simulation of Multibeam’s low-energy (5 keV) e-beam column design for the 45nm technology node as well as an analysis of its effect on rad-hard devices. Following its successful completion in early 2013, SMC funded a project to fabricate the first array of e-beam columns to confirm the essential capabilities of Multibeam’s design. The SMC project was successfully completed in late 2013.

Multibeam is currently working on two projects, both wrapping up in Q1 2016. In DTRA Phase II, Multibeam developed prototype electronics and software to vector-scan multiple e-beams. In AFRL Phase III, Multibeam developed a bench-top prototype system to demonstrate CEBL writing with a multi-column array in which all columns write independently and in parallel.

Multibeam is in discussion with Title III to build and ship an EBL production system to a Trusted fab. The work is comprised of two overlapping stages: In stage 1, Multibeam builds a production prototype system that demonstrates system functionality and performance. In stage 2, Multibeam builds and delivers an EBL production system to a Trusted fab.

Concurrently, a DTRA Phase III project is planned to develop 1D layout and CEBL process technology to support use of maskless EBL systems by Trusted fabs in the production of RHIC and other DoD microchips.

Acknowledgements

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References

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