Exhibit R-2, PB 2010 Defense Advanced Research Projects Agency RDT&E Budget Item Justification								DATE: May 2009		
APPROPRIATION/BUDGET ACTIVITY 0400 - Research, Development, Test & Evaluation, Defense-Wide/BA 2 - Applied Research					R-1 ITEM NOMENCLATURE PE 0602716E ELECTRONICS TECHNOLOGY					
COST ($ in Millions)	**FY 2008 Actual**	**FY 2009 Estimate**	**FY 2010 Estimate**	**FY 2011 Estimate**	**FY 2012 Estimate**	**FY 2013 Estimate**	**FY 2014 Estimate**	**FY 2015 Estimate**	**Cost To Complete**	**Total Cost**
Total Program Element	181.321	199.396	223.841						Continuing	Continuing
ELT-01: ELECTRONICS TECHNOLOGY	181.321	199.396	223.841						Continuing	Continuing

A. Mission Description and Budget Item Justification

(U) This program element is budgeted in the Applied Research budget activity because its objective is to develop electronic components, subsystems, and design tools that enable a wide range of military capabilities.

(U) Advances in microelectronic device technologies; including digital, analog, photonic and MicroElectroMechanical systems (MEMS) devices; continue to have significant impact in support of defense technologies for improved weapons effectiveness, improved intelligence capabilities and enhanced information superiority. The Electronics Technology program element supports the continued advancement of these technologies through the development of performance driven advanced capabilities, exceeding that available through commercial sources, in electronic, optoelectronic and MEMS devices. This also includes semiconductor device design and fabrication techniques, new materials and new material structures for device applications. A particular focus for this work is the exploitation of chip-scale heterogeneous integration technologies that permit the optimization of device and integrated module performance.

(U) The phenomenal progress advances in Transition density within microelectronic integrated circuits will face the fundamental limits of silicon technology in the early 21st century, a barrier that must be overcome in order for progress to continue. Another thrust of the program element will explore alternatives to silicon-based electronics in the areas of new electronic devices, novel/alternative materials, new architectures to utilize them, new software to program the systems, and new methods to fabricate the chips. Approaches include nanotechnology, nanoelectronics, molecular electronics, spin-based electronics, quantum-computing, photonics processing and computing; and new circuit, computer and electronic systems architectures. Projects will investigate the feasibility, design, and development of powerful information technology devices and systems using approaches to electronic device designs that extend beyond traditional Complementary Metal Oxide Semiconductor (CMOS) scaling, including non silicon-based materials technologies to achieve low cost, reliable, fast and secure computing, communication, and storage systems. This investigation is aimed at developing new capabilities from promising directions in the design of information processing components using both inorganic and organic substrates, designs of components and systems leveraging quantum effects and chaos, and innovative approaches to computing designs incorporating these components for such applications as low cost seamless pervasive computing, ultra-fast computing, and sensing and actuation devices. This project has five major thrusts: Electronics, Photonics, MicroElectroMechanical Systems (MEMS), Architectures, and Algorithms. Other core research will be pursued to ensure state-of-the-art military capabilities.

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B. Program Change Summary ($ in Millions)

	FY 2008	FY 2009	FY 2010	FY 2011
Previous President's Budget	196.707	211.457	229.195	
Current BES/President's Budget	181.321	199.396	223.841	
Total Adjustments	-15.386	-12.061	-5.354	
Congressional Program Reductions	0.000	-16.741		
Congressional Rescissions	0.000	0.000		
Total Congressional Increases	0.000	4.680		
Total Reprogrammings	-10.000	0.000		
SBIR/STTR Transfer	-5.386	0.000		
TotalOtherAdjustments			-5.354	

Congressional Increase Details ($ in Millions)	FY 2008	FY 2009
Project: ELT-01, **3-D Technology for Advanced Sensor Systems**	0.000	1.440
Project: ELT-01, **Indium Based Nitride Technology Development**	0.000	3.000
Project: ELT-01, **Secure Media and ID Card Development**	0.000	0.240

Change Summary Explanation

FY 2008
Decrease reflects the AFRICOM reprogramming and SBIR/STTR transfer.

FY 2009
Decrease reflects reductions for Section 8101 Economic Assumptions and new starts.

FY 2010
Decrease reflects minor rephasing of electronics technology programs.

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COST ($ in Millions)	**FY 2008 Actual**	**FY 2009 Estimate**	**FY 2010 Estimate**	**FY 2011 Estimate**	**FY 2012 Estimate**	**FY 2013 Estimate**	**FY 2014 Estimate**	**FY 2015 Estimate**	**Cost To Complete**	**Total Cost**
ELT-01: ELECTRONICS TECHNOLOGY	181.321	199.396	223.841						Continuing	Continuing

A. Mission Description and Budget Item Justification

(U) This program element is budgeted in the Applied Research budget activity because its objective is to develop electronics that make a wide range of military applications possible.

(U) Advances in microelectronic device technologies, including digital, analog, photonic and MicroElectroMechanical Systems (MEMS) devices, continue to have significant impact in support of defense technologies for improved weapons effectiveness, improved intelligence capabilities and enhanced information superiority. The Electronics Technology program element supports the continued advancement of these technologies through the development of performance driven advanced capabilities, exceeding that available through commercial sources, in electronic, optoelectronic and MEMS devices, semiconductor device design and fabrication techniques, and new materials and material structures for device applications. A particular focus for this work is the exploitation of chip-scale heterogeneous integration technologies that permit the optimization of device and integrated module performance.

(U) The phenomenal progress in current electronics and computer chips will face the fundamental limits of silicon technology in the early 21st century, a barrier that must be overcome in order for progress to continue. Another thrust of the program element will explore alternatives to silicon-based electronics in the areas of new electronic devices, new architectures to use them, new software to program the systems, and new methods to fabricate the chips. Approaches include nanotechnology, nanoelectronics, molecular electronics, spin-based electronics, quantum-computing, new circuit architectures optimizing these new devices, and new computer and electronic systems architectures. Projects will investigate the feasibility, design, and development of powerful information technology devices and systems using approaches for electronic device designs that extend beyond traditional Complementary Metal Oxide Semiconductor (CMOS) scaling, including non silicon-based materials technologies to achieve low cost, reliable, fast and secure computing, communication, and storage systems. This investigation is aimed at developing new capabilities from promising directions in the design of information processing components using both inorganic and organic substrates, designs of components and systems leveraging quantum effects and chaos, and innovative approaches to computing designs incorporating these components for such applications as low cost seamless pervasive computing, ultra-fast computing, and sensing and actuation devices. This project has five major thrusts: Electronics, Photonics, MicroElectroMechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

B. Accomplishments/Planned Program ($ in Millions)	**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
Advanced Microsystems Technology Program	5.000	5.000	5.000	

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
(U) The Advanced Microsystems Technology program will explore a range of advanced microsystem concepts well beyond existing current technologies. The program focuses on technologies that exploit 3-Dimensional (3-D) structures, new materials for Gieger mode detectors, advance patterning, and extreme scaling in silicon devices. Insights derived in these areas will be exploited in future program initiatives. These initiatives include advanced high-resolution lithography, high-speed avalanche devices with response out to 2 micrometers (um); integration of periodic elements III-V material with silicon; and novel cryogenic electronics. *FY 2008 Accomplishments:* - Demonstrated photoresist capable of multiple in-situ exposure with enhanced resolution. - Demonstrated sub-35 nanometer (nm) half-pitch interometric liquid exposure capability. *FY 2009 Plans:* - Prepare report analyzing prospects for beyond roadmap technologies. - Deliver data on ultra-low voltage operation of Silicon Complimentary Metal Oxide Semiconductor (CMOS) for DoD applications. *FY 2010 Plans:* - Demonstrate midwave IR (MWIR) photon-counting arrays using antimonide-based avalanche photodiodes. - Demonstrate nanolithography techniques, which enable use of electron-beam lithography in conjunction with interferometric optical patterning or templated self-assembly. - Demonstrate focal planes using dense monolithic 3-D integration of silicon electronics and compound semiconductor detectors. - Demonstrate ultra low-power silicon CMOS technology optimized for DoD applications such as space electronics, long endurance microsensors, and extreme temperature electronics.					
High Frequency Wide Band Gap Semiconductor Electronics Technology (U) The overall objective of the High Frequency Wide Band Gap Semiconductors Electronic Technology Initiative is to fully exploit the properties of wide bandgap semiconductors (WBGS) to enhance the		34.625	11.250	4.790	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
capabilities of microwave and millimeter-wave (MMW) monolithic integrated circuits (MMICs) and in turn, enable future RF sensor, communication, and multifunction military capabilities. Wide bandgap semiconductors have the ability to deliver very high power and other very favorable high frequency characteristics. Prior efforts have focused on improvements to the basic semiconductor while current efforts are focused on realizing devices and circuits. These technologies will lead to affordable, high performance, reliable, wide bandgap devices and MMICs with characteristics suitable for enabling new DoD systems and greatly improved performance for fielded platforms. *FY 2008 Accomplishments:* - Demonstrated epitaxial processes that yield + three percent uniformity over 75 mm wide bandgap substrates. - Initiated thermal management study to determine best packaging approach for high power, high frequency microwave and millimeter wave transistors. - Demonstrated 100 mm silicon carbide (SiC) and wide bandgap alternate substrates with less than 40 micropipe/cm squared and resistivity 10^7 power ohms-cm. - Demonstrated epitaxial processes that yield + one percent uniformity over 100 mm wide bandgap substrates. - Identified fabrication processes for robust microwave and mm-wave devices. *FY 2009 Plans:* - Identify thermal management concepts to sustain more than 1 KW/cm squared power density in high-power devices. - Optimize wide bandgap semiconductor materials to achieve 100 mm substrates with less than 10 micropipe/cm squared and resistivity greater than 10^7 ohms-cm at room temperature. - Demonstrate fabrication processes for robust microwave and mm-wave devices with radio frequency yields greater than seventy percent. - Demonstrate thermal management concepts to sustain more than 1 KW/cm squared power density in high power device.				

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
FY 2010 Plans: - Develop and utilize physics-based models that accurately predict device performance. - Demonstrate reproducible wide bandgap semiconductors (WBGS) device and monolithic integrated circuits (MMICs) fabrication processes. - Demonstrate WBGS devices and MMICs that, while maintaining high levels of producibility and reliability, achieve substantially higher levels of performance compared to GaAs-based microwave and microwave millimeter-wave (MMW) devices and MMICs. - Demonstrate superior thermal management and packaging strategies.					
High Power Wide Band Gap Semiconductor Electronics Technology (U) The High Power Wide Band Gap Semiconductor Electronics Technology developed components and electronic integration technologies for high power, high frequency microsystem applications based on wide bandgap semiconductors. *FY 2008 Accomplishments:* - Demonstrated megawatt Class silicon carbide (SiC) power devices. - Demonstrated high power density packaging for greater than 10 kV operations.		1.500	0.000	0.000	
Quantum Information Science (QIS) (U) The Quantum Information Science (QIS) program will explore all facets of the research necessary to create new technologies based on quantum information science. Research in this area has the ultimate goal of demonstrating the potentially significant advantages of quantum mechanical effects in communication and computing. Expected applications include: new improved forms of highly secure communication; faster algorithms for optimization in logistics and wargaming; highly precise measurements of time and position on the earth and in space; and new image and signal processing methods for target tracking. Technical challenges include: loss of information due to quantum decoherence; limited communication distance due to signal attenuation; limited selection of algorithms and protocols; and larger numbers of bits. Error correction codes, fault tolerant schemes, and longer decoherence times will address the loss of information. Signal attenuation will be overcome by exploiting		1.966	3.350	3.230	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
quantum repeaters. New algorithm techniques and complexity analysis will increase the selection of algorithms, as will a focus on signal processing. The QIS program is a broad-based effort that will continue to explore the fundamental open questions, the discovery of novel algorithms, and the theoretical and experimental limitations of quantum processing as well as the construction of efficient implementations. *FY 2008 Accomplishments:* - Investigated alternative designs, architectures and devices for quantum communication and demonstrated high-rate (1Gbit/sec) quantum-secure communication over a single link. *FY 2009 Plans:* - Investigate unresolved fundamental issues related to quantum information science. - Employ qubit architectures to demonstrate applications of interest to the DoD (e.g., quantum repeater, secure metropolitan-area network). - Demonstrate interoperation between multiple qubit types to interconnect quantum communications links. *FY 2010 Plans:* - Measure single electron spin lifetime and demonstrate controlled gate operations in gated quantum dots in silicon (Si). - Conduct theoretical analysis of improvement in decoherence time resulting from dynamical decoupling schemes. - Explore novel materials, noise characteristics and decoherence mitigation strategies for superconducting qubits.				
Submillimeter Wave Imaging Focal Plane Array (FPA) Technology (SWIFT) (U) The Submillimeter Wave Imaging Focal Plane Array (FPA) Technology (SWIFT) program developed revolutionary component and integration technologies to enable exploitation of this spectral region. A specific objective was the development of a new class of sensors capable of low-power, video-rate, background and diffraction limited submillimeter imaging.	1.046	0.000	0.000	

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B. Accomplishments/Planned Program ($ in Millions)	**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
FY 2008 Accomplishments: - Developed sensitive and large format receiver arrays, advanced integration, and backend signal processing techniques. - Developed and demonstrated a submillimeter focal plane imager.				
Technology for Frequency Agile Digitally Synthesized Transmitters (TFAST) (U) The Technology for Frequency Agile Digitally Synthesized Transmitters (TFAST) program (Ultra High-Speed Circuit Technology) developed super-scaled Indium Phosphide (InP) Heterojunction Bipolar Transistor (HBT) technology compatible with a ten-fold increase in transistor integration for complex mixed signal circuits. Phase I established the core transistor and circuit technology to enable the demonstration of critical small scale circuit building blocks suitable for complex mixed signal circuits operating at speeds three times that currently achievable and ten times lower power. Phase II extended the technology to the demonstration of complex (more than 20,000 transistors) mixed signal circuits with an emphasis on direct digital synthesizers for frequency agile transmitters. *FY 2008 Accomplishments:* - Developed full circuit capability using super-scaled InP HBTs in complex (more than 20,000 transistors) circuits. - Established device models and critical design rules. - Advanced the development of world's fastest InP HBT device technology.	7.391	0.000	0.000	
Feedback-Linearized Microwave Amplifiers (U) Modern military platforms require increased dynamic range receivers for their onboard communications in both radar and electronic warfare antenna systems. The goal of the Feedback-Linearized Microwave Amplifiers program is to develop radio frequency (RF) amplifiers with revolutionary increased dynamic range receivers through the use of linear negative feedback. This program will develop the core technologies and components that may be used as building blocks and/or modules in future system applications. This program will leverage technologies from the TFAST program.	5.360	3.910	2.650	

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
FY 2008 Accomplishments: - Developed indium phosphide (InP) Heterojunction Bipolar Transistor (HBT)-based ultra-high linearity low-noise amplifier circuit architecture and developed low-noise InP High Electron Mobility Transistor (HEMT) devices. *FY 2009 Plans:* - Develop and enhance InP HBT-based RF operational amplifier and InP HEMT-based ultra-low-noise amplifier. *FY 2010 Plans:* - Demonstrate feedback-linearized all-HBT monolithic low-noise amplifier with improved third-order-intercept point and noise factor. - Demonstrate feedback linearized InP HEMT monolithic low-noise amplifier. - Establish packaging technology for composite phase-III low-noise amplifier module.					
Terahertz Electronics* *Formerly Terahertz Imaging Focal-Plane Technology (TIFT). (U) Terahertz Electronics will develop the critical semiconductor device and integration technologies necessary to realize compact, high-performance microelectronic devices and circuits that operate at center frequencies exceeding 1 Terahertz (THz). There are numerous benefits to operating in the THz regime and multiple new applications in imaging, radar, communications, and spectroscopy, all enabled by electronics that operate in the THz frequency regime. The Terahertz Electronics program is divided into two major technical activities: Terahertz Transistor Electronics that includes the development and demonstration of materials and processing technologies for transistors and integrated circuits for receivers and exciters that operate at THz frequencies; and Terahertz High Power Amplifier (HPA) Modules that includes the development and demonstration of device and processing technologies for high power amplification of THz signals in compact modules.		5.260	11.000	11.980	

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B. Accomplishments/Planned Program ($ in Millions)	**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
FY 2008 Accomplishments: - Demonstrated a compact THz source achieving at least 10 mW of average power and one percent wall plug efficiency, as required for active illumination and/or for local oscillators in heterodyne or homodyne detection schemes. *FY 2009 Plans:* - Develop devices and circuits for candidate applications with demonstration of operation at a frequency of at least 0.67 THz. - Demonstrate 18dBm power amplification at 0.67 THz. *FY 2010 Plans:* - Develop devices and circuits for candidate applications with demonstration of operation at a frequency of at least 0.85 THz. - Demonstrate 14dBm power amplification at 0.85 THz.				
Trusted, Uncompromised Semiconductor Technology (TrUST) (U) The Trusted, Uncompromised Semiconductor Technology (TrUST) program addresses the fundamental problem of determining whether a microchip manufactured through a process that is inherently “untrusted” (i.e., not under our control) can be “trusted” to perform operations only as specified by the design, and no more. The program consists of a set of complementary technologies integrated together in order to develop a product that could be transitioned to the DoD. The TrUST program has moved to Program Element 0602303E, Project IT-03 in FY 09 and out as the program focuses on "trusted" hardware and software validation. *FY 2008 Accomplishments:* - Demonstrated automated Focus Ion Beam (FIB) delayering, Scanning Electron Microscope (SEM) imaging, and image processing to reconstruct the Integrated Circuit (IC) Gieber Data Standard (GDSII) from SEM images. - Developed automated algorithms for inspecting the Register Transfer List (RTL)-to-Netlist and Netlist-to-GDS components of the design flow for the protection of the IC design files.	19.281	0.000	0.000	

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
- Created techniques to associate logic cell libraries with functional characteristics provided in 3rd Party Intellectual Property (IP) specifications in Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs) for the protection of 3rd Party IP blocks. - Developed techniques to ensure that the bit-stream accurately represents what was originally designed in the RTL description for protection of FPGA program files. - Developed Physically Unclonable Functions to authenticate FPGAs to protect FPGAs from substitutions.					
Carbon Electronics for RF Applications (CERA) (U) The CERA program will develop a wafer-scale graphene (2-Dimensional carbon monolayer) synthesis process resulting in films with excellent mobility, uniformity and layer control (down to single monolayer films). These carbon films will then be used to develop ultra-low power, high-speed field effect transistors optimized for RF-applications (RF-FET). The program will conclude with a demonstration of a low power, low noise amplifier (LNA) using graphene-field effect transistors (FETs) as the channel material. *FY 2008 Accomplishments:* - Demonstrated hybrid graphene-silicon complimentary metal-oxide semiconductor (CMOS) circuits for high performance and low power applications. *FY 2009 Plans:* - Develop synthesis process for wafer-scale graphene thin films. - Demonstrate feasibility of graphene channel based FETs. *FY 2010 Plans:* - Optimize synthesis process for wafer-scale graphene thin films. - Optimize RF-FETs based on graphene channels.		8.167	7.146	7.525	
Compound Semiconductor Materials On Silicon (COSMOS) (U) The objective of the Compound Semiconductor Materials On Silicon (COSMOS) program is to develop a robust semiconductor fabrication technology and manufacturing process for the intimate		1.589	18.040	12.519	

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**

integration of multiple types of devices and semiconductor materials. Conventional semiconductor processing is limited to one type of semiconductor but most DoD systems have circuits with multiple types of semiconductor circuits and devices. This program is developing heterogeneous material and device fabrication technologies to allow compound semiconductors to be directly integrated with standard silicon. The high yield fabrication approaches will allow the various materials to be in close proximity. This program is also focusing on innovations in design to ensure that the resulting composite circuits realize superior performance in advanced circuit demonstrations.

FY 2008 Accomplishments:
- Developed methods for sub-circuit integration onto fully processed complimentary metal-oxide semiconductor (CMOS) wafers.
- Developed scalable electro-magnetic (EM), thermal and mechanical models.
- Estimated thermal and mechanical properties of integration materials, performed thermal and stress modeling to determine and improve the viability of the COSMOS thermal and mechanical design.

FY 2009 Plans:
- Fabricate wafers using the COSMOS process.
- Evaluate alignment and bonding methods to achieve mechanical integrity of dissimilar materials, post-processing compatibility with CMOS, and the achievement of high fabrication yields.
- Extend the capabilities of wide bandgap devices for use in power amplifiers (PAs) at frequencies at least as high as X-band and to make this technology useful at very high frequencies.
- Demonstrate large (greater than 1 mm) devices.
- Decrease the number of optical phonons in the critical gate region of radio frequency (RF) PA devices.

FY 2010 Plans:
- Increase the density of heterogeneous interconnections between compound semiconductors and silicon.
- Implement process enhancements to improve the yield of the heterogeneous interconnect process.
- Complete design of an advanced mixed-signal circuit demonstrator such as a heterogeneously-integrated 13-bit digital-to-analog converter.

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
Steep-subthreshold-slope Transistors for Electronics with Extremely-Low Power (STEEP)	3.424	5.306	9.080	

(U) The Steep-subthreshold-slope Transistors for Electronics with Extremely-low Power (STEEP) program goal is to develop revolutionary transistor technologies, which enable devices to be operated at voltages as low as 0.2 V without loss in performance (defined by available drive current). The approach is to develop novel transistors with sub-threshold “turn-on” slopes as sharp as 20 millivolt (mV)/decade while maintaining excellent current drive characteristics. This program will mainly focus on developing band-to-band tunneling transistors that will be operated at low bias voltages with high saturation current and low leakage current. In addition, associated device models will also be developed in the program to enable novel ultra-low power circuit designs. At the end of the program, complex demonstration circuits will achieve significant power savings, both active and standby, of at least twenty-five times. The STEEP transistors will utilize the mechanism of gate controlled modulation of the energy band alignment between the conduction and valence bands of a band-to-band-tunneling device. The key technical challenges of the program will include (1) achieving steep sub-threshold slope over many decades of current, (2) developing CMOS compatible fabrication flow, (3) developing novel circuit designs accommodating asymmetric source-drain doping, (4) demonstrating abrupt doping profiles at tunneling junctions, and (5) integrating silicon-germanium (SiGe), germanium (Ge), or group III-V material in the transistor structures to facilitate the required tunneling currents. The STEEP program will start with the development of transistors with less than 30mV/dec of sub-threshold slope and then proceed to demonstrate the integration of these devices into logic circuits using an eight inch wafer technology. Finally, the STEEP program will focus on the yield improvement of a complex ultra-low power static random access memory (SRAM) circuit.

FY 2008 Accomplishments:
- Developed transistors with 30 mV/dec of subthreshold slope.

FY 2009 Plans:
- Develop associated device models of band-to-band tunneling transistors.
- Engineer transistor structures and begin fabrication of key device modules capable of meeting performance milestones of low power consumption and good performance.

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
FY 2010 Plans: - Further optimize the STEEP transistor performance and models. - Develop integrated fabrication processes capable of producing transistors and basic circuits. - Validate ultra-low power performance using a ring oscillator and a static random access memory (SRAM).					
High Frequency Integrated Vacuum Electronic (HiFIVE)* *Formerly titled Compact Vacuum Electronic Radio-Frequency Technology (COVERT). (U) The objective of the High Frequency Integrated Vacuum Electronic (HiFIVE) program is to develop and demonstrate new high-performance and low-cost technologies for implementing high power millimeterwave sources and components. This program is developing new semiconductor and micro-fabrication technologies to produce vacuum electronic (VE) high-power amplifiers (HPA) for use in high-bandwidth, high-power transmitters. Innovations in design and fabrication are being pursued to enable precision etching, deposition, and pattern transfer techniques to produce resonant cavities, electrodes, and magnetics, and electron emitting cathodes for compact high-performance millimeter wave devices. These new technologies will eliminate the limitations associated with the conventional methods for assembly of high-power sources in this frequency range. *FY 2008 Accomplishments:* - Demonstrated a high aspect ratio beam with required power and transport efficiency. *FY 2009 Plans:* - Validate cold test interaction of structure design and high current density cathode. - Explore/identify novel material to optimize circuit performance characteristics. *FY 2010 Plans:* - Validate the design of a high power amplifier through experiments and computational simulation. - Complete development of the high-performance cathode prototype and demonstrate its ability to operate without degradation for at least 1000 hours.		5.693	9.090	8.430	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
Semiconductor-Tuned HTS Filters for Ultra-Sensitive RF Receivers (SURF)	4.577	4.042	4.000	

(U) The operation of frequency-hopping radios greatly interferes with co-located ultra-sensitive receivers. The situation will get worse as the “hoppers” proliferate, even interfering within the receive channels of one another. At present there is no solution to this problem, other than turning off the receivers when communicating. A general solution would be to use “brick-wall” front-end filters for the receivers, retuning at the rate of the hoppers, if such agile filters were available. High-temperature superconducting (HTS) filters have been used very successfully for negating strong transmissions at nearby frequencies, and are unique in their ability to totally reject out-of-band signals without attenuation of signals in the pass-band. However, they have been used only for rejection of fixed-frequency interference.

(U) The Semiconductor-Tuned HTS Filters for Ultra-Sensitive RF Receivers (SURF) program will increase the tuning speed of HTS filters, from about a second with present mechanical methods, to microsecond speeds required for systems such as the Joint Tactical Information Distribution System (JTIDS). The technology for such a million-fold improvement relies upon semiconductor tuning, properly mated with the superconducting filter materials. In addition to interference-rejection at microsecond speeds, these filters make it possible to perform wide spectral searches with unprecedented frequency resolution, enabling detection of very weak emissions (signatures) characteristic of threat systems.

FY 2008 Accomplishments:
- Demonstrated one microsecond switching of high-temperature superconducting (HTS) filters, between three frequencies.
- Developed models of the HTS tunable filters.
- Achieved microsecond stepwise semiconductor switching between three stable states.

FY 2009 Plans:
- Continue development of low-loss semiconductor tuning elements for HTS filters, operating at cryogenic temperatures.

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
FY 2010 Plans: - Complete development of low-loss semiconductor tuning elements for HTS filters, operating at cryogenic temperatures.					
Adaptive Focal Plane Arrays (AFPA) (U) The goal of the Adaptive Focal Plane Arrays (AFPA) program is to demonstrate high-performance focal plane arrays that are widely tunable across the entire infrared (IR) spectrum (including the short-, middle- and long-wave IR bands), thus enabling "hyperspectral imaging on a chip." This program will also enable broadband Forward Looking Infrared (FLIR) imaging with high spatial resolution. These AFPAs will be electrically tunable on a pixel-by-pixel basis, thus enabling the real-time reconfiguration of the array to maximize either spectral coverage or spatial resolution. The AFPAs will not simply be multi-functional, but rather will be adaptable by means of electronic control at each pixel. Thus, the AFPAs will serve as an intelligent front-end to an optoelectronic microsystem. The AFPA program outcome will be a large format focal plane array that provides the best of both FLIR and Hyper-Spectral Imaging (HSI). *FY 2008 Accomplishments:* - Integrated detector array. - Demonstrated pixel-by-pixel electrical tunability in infrared. *FY 2009 Plans:* - Demonstrate AFPA prototype field using a large format array.		2.920	1.275	0.000	
Chip-to-Chip Optical Interconnects (C2OI) (U) Continuing advances in integrated circuit technology are expected to push the clock rates of Complimentary Metal-Oxide Semiconductor (CMOS) chips into 10 gigahertz (GHz) range over the next five to seven years. At the same time, copper-based technologies for implementing large number of high-speed channels for routing these signals on a printed circuit board and back planes are expected to run into fundamental difficulties. This performance gap in the on-chip and between-chip interconnection technology will create data throughput bottlenecks affecting military-critical sensor signal processing		2.700	3.112	3.025	

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
systems. To address this pressing issue, this program is developing optical technology for implementing chip-to chip interconnects at the board and back plane level. *FY 2008 Accomplishments:* - Integrated optical transmitters/receivers and optical data paths with electronic packaging. *FY 2009 Plans:* - Develop a chip-scale opto-electronic transceiver circuit based on C2OI technology and demonstrate operation equivalent to 1 Terabit per second (Tbit/s) (consisting of twenty-four bidirectional channels each operating at 20 Gigabits/second (Gb/s)). - Develop a chip-scale opto-electronic transceiver consisting of twelve bidirectional channels each operating at 15 Gb/s that is fully integrated with commercially manufactured circuit boards. *FY 2010 Plans:* - Initiate efforts to complete a full system-scale demonstration of the use of C2OI technology approaches through the optical interconnect of two high performance computer servers using embedded C2OI technology with commercial circuit boards. - Complete a Technology/Manufacturing Readiness Assessment for C2OI technology with respect to commercial supercomputing and military high-performance embedded computing environments.					
Photonic Analog Signal Processing Engines with Reconfigurability (PhASER) (U) The goal of the Photonic Analog Signal Processing Engines with Reconfigurability (PhASER) program is the creation of new Photonic Integrated Circuit (PIC) elements, and associated programmable filter array concepts that will enable high-throughput, low-power signal processors. The focus is on the development of novel “Unit Cells,” which may be used as building blocks to synthesize arbitrarily complex filters within a PIC platform for ultra-high bandwidth signal processing applications. *FY 2008 Accomplishments:* - Defined and designed a novel analog photonic “Unit Cell” that was nominally comprised of a sub-array of waveguide-connected programmable active elements.		3.496	3.980	0.000	

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- Demonstrated that the Unit Cell was externally linkable with integrated waveguides, and could function as a building block in programmable PIC arrays for generalized high-order finite impulse response/infinite impulse response (FIR/IIR) filters. *FY 2009 Plans:* - Demonstrate an experimental Unit Cell concept. - Determine how the Unit Cell, when arrayed within a high-density PIC, will perform. - Develop a filter synthesis tool to demonstrate how Unit Cells will enable generalized high-order filters. - Determine how unit cells will be programmed and tested at the chip-level to ensure high yield.				
Linear Photonic RF Front End Technology (PHOR-FRONT) (U) The goal of the Linear Photonic RF Front End Technology (PHOR-FRONT) program is to develop photonic transmitter modules that can adapt their frequency response and dynamic range characteristics to mate with the full spectrum of narrow-band and broadband microwave transmission applications covering the 2 Megahertz (MHz) – 20 Gigahertz (GHz) range. These field programmable, real-time adaptive photonic interface modules will find application in high dynamic range communications, radar and Electronic Warfare antenna applications. *FY 2008 Accomplishments:* - Developed narrow line-width, 1,550 nanometer (nm) lasers with improved efficiency, relative intensity noise (RIN), and stability. *FY 2009 Plans:* - Develop compact linear photonic receivers with improved sensitivity and dynamic range.	7.238	2.875	0.000	
Optical Arbitrary Waveform Generation (OAWG) (U) The ultimate vision for the Optical Arbitrary Waveform Generator (OAWG) program is to demonstrate a compact, robust, practical, stable octave-spanning optical oscillator, integrated with an encoder/decoder capable of addressing individual frequency components with an update rate equal to the mode-locked repetition rate. This would provide an unprecedented level of performance for optical systems, and enable	0.964	4.284	0.000	

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
numerous high-level applications including sub-diffraction-limited imaging and ultra-wide band optical communications. *FY 2008 Accomplishments:* - Continued to develop 10 Gigahertz (GHz) octave-spanning carrier-envelope stabilized laser with integrated molecular frequency standard. - Continued to design and build miniature 10 Gigabyte/second multi-channel, parallel bit-error rate testbed for integrated system testing. *FY 2009 Plans:* - Demonstrate 1,000 GHz positive linear chirp with less than five percent least-squared deviation from mathematical ideal waveform. - Demonstrate production of single-cycle, 3 GHz square wave with fidelity of less than one percent least-squared deviation from mathematical ideal waveform. - Investigate insertion of OAWG technology into high performance radar and laser radar systems.					
Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) (U) The Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) program will develop a brain inspired electronic “chip” that mimics the function, capacity, size, and power consumption of a biological cortex. If successful, the program will provide the foundations for functional machines to supplement humans in many of the most demanding situations faced by warfighters today. In particular, the objective of the program is to process video images for information abstraction (e.g. annotation) and task initiation. The two main technical challenges to achieving this vision are developing an artificial electronic synapse and developing a neural algorithm-architecture that exploits these synapses. *FY 2008 Accomplishments:* - Initiated development of video image processing for information abstraction.		4.652	21.486	22.361	

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
FY 2009 Plans: - Develop a nanometer scale electronic synapse exhibiting the critical communication, processing and learning functions of biological synapses. - Develop microcircuit architecture employing hybrid complementary metal oxide semiconductor (CMOS) and high-density electronic synapses to replicate core functions of lower-level biological neural systems. *FY 2010 Plans:* - Develop a brain-inspired neuromorphic architectural design and specification capability. - Develop software tools to translate neuromorphic designs into electronic implementations using hybrid CMOS and high-density electronic synapse components. - Develop capability to simulate the performance of neuromorphic electronics systems using very large scale computation. - Develop virtual reality environments intended for training and evaluating electronic neuromorphic systems and their corresponding computer simulations. - Develop standard testing protocols for assessing the performance of large neuromorphic electronic systems.					
Ultrabeam (U) The goal of the Ultrabeam program is to demonstrate the world's first gamma-ray laser using laboratory equipment. The demonstration of an X-ray laser with photon energies of 4-5 thousand electron volts (KeV) (Xenon laser at 2-3 Angstrom wavelengths) in the first phase of the Ultrabeam program opens the possibility of creating gamma-ray lasers with photon energies equivalent to 100 KeV – 1 million electron volts (MeV). Compact gamma ray lasers can enable the development of new and more effective radiation therapies and radiation diagnostic tools for medical and materials/device inspection applications. This unique X-ray laser technology could also eventually enable the development of compact, laboratory-scale high-brightness coherent sources for 3-Dimensional molecular scale imaging of living cells and debris-free advanced lithography. *FY 2008 Accomplishments:* - Identified candidate gamma ray gain systems.		2.188	3.419	2.647	

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
- Obtained evidence for X-ray beam collapse in solid targets. - Analyzed new laboratory equipment including a new highly reliable ten times brighter Excimer Pre-Amp Laser with high beam to enable more efficient coupling of greater pump powers into the X-ray laser amplification channel for scaling of the X-ray laser output. *FY 2009 Plans:* - Demonstrate excitation of inner shell and nuclear levels in candidate gamma ray gain media. - Demonstrate modeled gain of greater than 50 cm^-1 in high atomic-number (Z greater than 70) candidates. - Estimate X-ray source scaling limits and source requirements for candidate gamma ray gain systems. - Demonstrate 50 milli Joule (mJ), 0.03 femtosecond (fs) X-ray laser output pulse. *FY 2010 Plans:* - Demonstrate gamma-ray amplification with a gain of greater than 100 cm^-1.					
Photonic Bandwidth Compression for Instantaneous Wideband A/D Conversion (U) The objective of the Photonic Bandwidth Compression for Instantaneous Wideband A/D Conversion (PHOBIAC) program is to develop revolutionary technologies to enable Analog to Digital Converters (ADCs) with high-resolution and large instantaneous bandwidth while maintaining power consumption that is commensurate with user community requirements. It is expected that such ADCs would have a dramatic impact on signals intelligence capabilities such as direct down conversion of ultra high frequency through X-band radio frequency (RF) signals. Furthermore, ADCs enabled by this program alleviate the current ADC bottleneck in high capacity digital RF communications links by enabling more spectrally efficient wideband waveforms. This program aims to develop a bandwidth-compressing photonic front end that provides a force multiplier for any available back-end electronic ADCs. *FY 2008 Accomplishments:* - Demonstrated transient ADC with 6.5 estimated number of bits (ENOB) signal-to-noise ratio over a 10 gigahertz bandwidth. - Developed a low-power ADC with high-dynamic range for an improved ENOB.		2.312	4.057	3.525	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
FY 2009 Plans: - Develop and enhance a low-power ADC with high-dynamic range for further improvement in the ENOB. *FY 2010 Plans:* - Develop a low-power ADC with enhanced ENOB and spurious-free dynamic range. - Develop and fabricate optical elements with high dispersion and low loss. - Investigate methods to improve noise performance of mode-locked laser systems while maintaining or improving output power and wall-plug efficiency.				
Optical Antenna Based on Nanowires (U) This program evaluated nano-meter scale structures that could act as optical antenna arrays that would respond coherently to electromagnetic fields at optical wavelengths. A system based on this technology would potentially be smaller, lighter in weight, and able to move from the sub-optimal method of intensity-only measurements into the information-rich domain of complex imaging. *FY 2008 Accomplishments:* - Completed a study on small element count 2-Dimensional array to identify performance and scaling relationships.	1.000	0.000	0.000	
Chip Scale Atomic Clock (CSAC) (U) The Chip Scale Atomic Clock (CSAC) will demonstrate a low-power chip scale atomic-resonance-based time-reference unit with stability better than one part per billion in one second. Application examples of this program will include the time reference unit used for Global Positioning System (GPS) signal locking. *FY 2008 Accomplishments:* - Demonstrated subcomponent fabrication including atomic chamber, excitation and detection function.	4.519	3.471	0.000	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
FY 2009 Plans: - Demonstrate design and fabrication innovation for atomic-confinement cell and for gigahertz (GHz) resonators suitable for phase locking or direct coupling with atomic confinement cell.				
Radio Isotope Micro-Power Sources (RIMS) (U) The Radio Isotope Micro-Power Sources (RIMS) effort will develop the technologies and system concepts required to safely produce electrical power from radioisotope materials for portable and mobile applications, using materials that can provide passive power generation. There will also be research in compact radioisotope battery approaches that harness MicroElectroMechanical Systems (MEMS) technology to safely and efficiently convert radioisotope energy to either electrical or mechanical power while avoiding lifetime-limiting damage to the power converter caused by highly energetic particles (e.g., such as often seen in previous semiconductor approaches to energy conversion). The goal is to provide electrical power to macro-scale systems such as munitions, unattended sensors, and weapon systems, radio frequency identification tags, and other applications requiring relatively low (up to tens of milliwatts) average power. *FY 2008 Accomplishments:* - Demonstrated advances in power output and particle capture with high conversion efficiencies, while operating within safety considerations and limitations. *FY 2009 Plans:* - Demonstrate advanced dielectrics with high stability suitable for solid-state capture devices. *FY 2010 Plans:* - Demonstrate long lasting power generation in a militarily useful form factor.	1.946	1.000	1.000	
Micro Isotope Micro-Power Sources (MIPS) (U) The goal of the Micro Isotope Micro-Power Sources (MIPS) program was to demonstrate safe, affordable micro isotope power sources able to outperform conventional batteries in terms of energy and/or power density, and provide long lasting milliwatt-level power for an array of critical military	7.664	0.000	0.000	

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
applications, such as unattended sensors, perimeter defense, detection of weapons of mass destruction; and environmental protection. *FY 2008 Accomplishments:* - Demonstrated radiation hardened Boron Carbide (BC) junctions with greater than ten percent efficiency. - Demonstrated thermophotovoltaic conversion system. - Demonstrated thermo electric conversion system.					
Novel Technologies for Optoelectronics Materials Manufacturing (NTOMM) (U) The goal of the Novel Technologies for Optoelectronics Materials Manufacturing (NTOMM) program is to develop and demonstrate new technologies for Group II-VI (e.g., Cadmium Selenide (CdSe)) and III-V (e.g., Gallium Nitride (GaN)) materials and device manufacturing, enabling imaging and emissive device fabrication at one percent to ten percent of current costs. This advance will dramatically expand the application space of such devices, by providing lower cost per large area infrared (IR) imaging systems, non-planar devices and systems, and thin film and flexible devices and systems. This program will demonstrate IR detectors and imagers, Light Emitting Diodes (LED), and solid-state lasers fabricated via new methods, and include a rapid demonstration of at least five times reduction in yielded device cost. The NTOMM program will leverage recent and ongoing developments in nano-material synthesis and assembly, which have demonstrated the potential for over fifty percent precursor stream usage in the fabrication of II-VI and III-V materials. An additional focus of the NTOMM program is the development of technologies to support the fabrication of low-cost high pixel density power efficient direct emission microdisplays. Current microdisplay systems use light modulation systems (Liquid Crystal Displays, Digital Micromirror Devices) and consequently only transmit a small fraction of the light from the illumination source thus limiting efficiency and use. *FY 2008 Accomplishments:* - Began development of cost effective synthesis methods for Group II-VI and III-V materials. - Developed higher temperature processing methods and hardware to provide better quality crystalline GaN.		3.750	3.000	2.500	

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B. Accomplishments/Planned Program ($ in Millions)	**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
FY 2009 Plans: - Develop and demonstrate techniques for layer doping of heterostructure materials. - Demonstrate fabrication technologies that support the fabrication of affordable emissive microdisplays. - Extend novel fabrication techniques to demonstrate initial device concepts. - Grow monodrystalline p-type GaN material with biased target based deposition based manufacturing process. - Demonstrate lift-off and substrate recycling. - Identify process optimization paths for improved material characteristics and expanded potential suite of low-cost devices that can be fabricated. *FY 2010 Plans:* - Demonstrate scalability of novel manufacturing techniques.				
Cognitively Augmented Design for Quantum Technology (CAD-QT) (U) The Cognitively Augmented Design for Quantum Technology (CAD-QT) program will enable rapid design, prototyping, and high-yield manufacture of next generation electronic, photonic, and magnetic devices that fully exploit quantum effects. One foundation of modern semiconductor electronics is that numbers of electronic carriers (electrons and holes) is large and this allows designers to rely on simple, semi-classical statistical models. As device dimensions become progressively smaller, quantum effects can no longer be treated as semi-classical statistical events and a complete and detailed quantum representation must be utilized. However, from the perspective of the human designer, quantum mechanics without statistical models is highly counterintuitive. The CAD-QT program will apply advances in robust optimization, dimensionality reduction, and modeling build tools for enhancing designer intuition for complex quantum systems optimized for high function and high yield under manufacturing variations. *FY 2008 Accomplishments:* - Extended CAD-QT quantum electronic device modeling and optimization tool for 3-Dimensional device structure.	1.339	5.000	5.500	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
FY 2009 Plans: - Develop optimization tools with automated search algorithms for heterojunction bipolar transistors (HBTs) operating in the 500 GHz to 1 THz region. *FY 2010 Plans:* - Optimize design and develop maskset design for ultra-high frequency HBT device.				
Ultra-Low Power Subthreshold Electronics (UPSE) (U) The Ultra-Low Power Subthreshold Electronics (UPSE) program will achieve a greater than ten times reduction in energy consumption for integrated circuits by developing technology that allows for circuit operation at the physical limits of power supply voltages. The objective of the UPSE program is to develop a circuit technology that will allow operation of devices in the subthreshold regime (less than or equal to 0.3 V) in contrast to the typical super-threshold regime (equivalent to 1.0 V). Particular emphasis is placed on the use of standard commercial complementary metal-oxide-semiconductor (CMOS) technology avoiding the need for specialized custom device fabrication. Application-specific parallelism will be leveraged for maintaining adequate performance in the sub-threshold regime while still consuming minimal power. A demonstration sensor or communication integrated circuit (IC) of significant military interest showing compelling low power performance and new mission capabilities will be built. *FY 2009 Plans:* - Develop standard cell digital design library that is capable of operating in subthreshold, near threshold and superthreshold voltage regimes. - Demonstrate highly efficient on-chip dc-dc converter for voltages less than 1 V. - Determine appropriate “granularity” of voltage/threshold domains in a digital IC for optimum low-power performance. *FY 2010 Plans:* - Design digital IC demos of DoD interest using low power libraries. - Fabricate several demo designs using advanced commercial foundry CMOS process. - Develop on-chip adaptive bias/threshold control scheme with fine-grained voltage domains.	0.000	6.361	6.000	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
Short-range Wide-field-of-regard Extremely-agile Electronically-steered Photonic Emitter and Receiver (SWEEPER) (U) The objective of the Short-range Wide-field-of-regard Extremely-agile Electronically-steered Photonic Emitter and Receiver (SWEEPER) program is to develop chip-scale dense waveguide modular technology to achieve true embedded phase array control for beams equivalent to 10W average power, less than 0.1 degree instantaneous field of view (IFOV), greater than 45 degree total field of view (TFOV), and frame rates of greater than 100 Hertz (Hz) in packages that are “chip-scale.” Such performance will represent a three order of magnitude increase in speed, while also achieving a greater than two orders of magnitude reduction in size. Additionally, the integrated phase control will provide the unprecedented ability to rapidly change the number of simultaneous beams, beam profile, and power-per-beam, thus opening a whole new direction in operational capability. Key technical challenges include the ability to achieve the needed facet density (facet pitch should be on the order of a wavelength or two), control the relative phase across all facets equivalent to 9-bits, and efficiently couple and distribute coherent light to facets from a master laser oscillator with an integrated waveguide structure. Related projects and studies have pointed to the significant system-level pay-offs of the new proposed technology. *FY 2009 Plans:* - Create a chip-scale optical beam forming and scanning technology. - Combine architecture and technology to address integrated control of phased optical signals. *FY 2010 Plans:* - Demonstrate chip scale beam-forming capability in laboratory. - Evaluate transmit and receive photonic phased array technologies.	0.000	4.000	7.500	
Analog-to-Information (A-to-I) (U) The Analog-to-Information (A-to-I) program will leverage recent dramatic breakthroughs in digitization techniques and hardware to enable accurate extraction of useful information from broadband environments crowded with diverse signals and interference spread over a large dynamic range. The program will satisfy DoD’s requirements for radio frequency (RF) applications of the present and the future. Additionally, by extracting signals of interest during the measurement phase, A-to-I based approaches	2.869	5.970	8.910	

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
reduce the bandwidth and resolution requirements of analog-to-digital converters, and simultaneously reduce the data glut that impacts downstream processing of digitized signals. *FY 2008 Accomplishments:* - Organized industry and academic teams to develop A-to-I receiver designs that address challenging DoD RF application scenarios. - Formulated, finalized, and established detailed simulation studies. *FY 2009 Plans:* - Systematically exploit practical hardware and software implementations of the most promising approaches from study phase: compressive sampling, variable projective unfolding, and nonlinear affine encoders. *FY 2010 Plans:* - Prototype critical hardware components of the design in order to avoid risk early; models based on performance measurements of these components will be incorporated into the simulation of the overall receiver.					
Computational Imaging (CI) (U) The Computational Imaging (CI) program will develop new imaging constructs that exploit the full information content (intensity, phase, and frequency) at the detection plan to perform real-time image processing in the analog domain. This will be combined with advanced digital image processing algorithms to leverage the unique image plane information for more rapid image analysis and target identification. This will lead to revolutionary advances in the detection, precision identification, tracking and destruction of elusive targets. *FY 2009 Plans:* - Begin the prototype development of a practical 3-Dimensional (3-D) spatial imager that captures intensity, frequency, and phase information of naturally illuminated scenery.		0.000	3.000	7.000	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
FY 2010 Plans: - Demonstrate prototype 3-D spatial imager with associated spatial processing algorithms.				
Electric Field Detector (E-FED)* *Formerly titled Non-contact EEG Technologies (NET). (U) The goal of the Electric Field Detector (E-FED) program is to develop a small room temperature electric field sensor/sensor array based on new optical electric field sensor architectures. Electric fields are ubiquitous in the warfighter environment. It is expected that these compact sensor arrays will be useful for the monitoring of brain activity and muscle action without the need to apply electrodes directly in or on the surface of the skin. The arrays would also be useful for the remote sensing of electronics, motors, and communications devices enabling the sensing of these devices at greater distances with a more unobtrusive and portable system. *FY 2009 Plans:* - Develop electric field sensors that utilize the modification of optical fields due to the presence of an electric field. *FY 2010 Plans:* - Explore techniques to control the effect of noise sources on the sensor function. - Demonstrate sensors sensitive to an alternating electric field of 1 million volts (mV)/mHz^1/2 from 1-10,000 Hertz (Hz). The sensor would have a dynamic range of 100 and a footprint size of no greater than 25 mm^2.	0.000	3.000	6.000	
Integrated Photonic Delays (iPhoD)* *Formerly titled Ultra Low Loss Photonic Integrated Circuits and Processors. (U) The Integrated Photonic Delays (iPhoD) program will enable unprecedented integrated optical delay performance and complexity, thereby furthering the technological precision of our military. The iPhoD program will build the framework of a scalable integrated photonic platform technology that provides for	0.000	3.000	6.000	

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
the handling and manipulation of photons with throughput efficiency and precision approaching that of electrons within electronic integrated circuits. *FY 2009 Plans:* - Demonstrate a minimum, on-chip, optical time delay of 100 nanoseconds (ns). *FY 2010 Plans:* - Refine waveguide materials, fabrication and coupling approaches. - Demonstrate a precise and low loss fiber input/output coupling technology.					
Processing Algorithms with Co-design of Electronics (PACE) (U) The Processing Algorithms with Co-design of electronics (PACE) program enables the co-design of the next generation of embedded signal processing algorithms and architectures capable of processing large sparse matrix data structures associated with graph structured signal processing algorithms. Graph algorithms are the key to post-detection signal processing, helping us “connect the dots” in a huge variety of emerging challenges ranging from network analysis, change detection in massive sensor data transactions, and forensic and predictive analyses of activities from video data over wide areas and extended times. The goal of the PACE program is to provide the DoD with an architecture and algorithm co-design capability for performing Graph-structured signal processing. Solutions available today that might meet these mission requirements are limited by prohibitively long and costly manual design times. The PACE program will provide signal processing capabilities not possible today while achieving dramatically reduced design time and cost. *FY 2009 Plans:* - Develop preliminary computational architectures that are optimized for processing of complex graph algorithms. - Begin implementation of microprocessor emulators.		0.000	3.000	5.000	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
FY 2010 Plans: - Demonstrate a better than ten time improvement of emulated processor over similar graph algorithms implemented on conventional Von Neumann computer platforms. - Develop co-design capability for hardware and software data analysis.				
Visible InGan Injection Lasers (VIGIL) (U) The objective of the Visible InGan Injection Lasers (VIGIL) program is to demonstrate injection lasers emitting in the green wavelength. The specific program goal is to demonstrate continuous wave green injection lasers operating at room temperature with a power output up to 1 watt, wall plug efficiency of thirty percent, and laser output stability over time periods of at least 1000 hours. VIGIL lasers will enable applications requiring a close match between the wavelength of the light source and the peak response wavelength of the human eye. Another class of applications will take advantage of the minimum absorption of seawater in the blue-green spectral region. Other applications include miniaturized displays and pumps for generation of high-frequency mode-locked combs. *FY 2008 Accomplishments:* - Demonstrated watt-level Indium Gallium Nitride (InGaN)-based injection lasers emitting in the visible wavelengths of 460-520 nanometers (nm). - Demonstrated optically pumped stimulated emission at 512 nm wavelength on a semi-polar semiconductor substrate. *FY 2009 Plans:* - Grow InGaN quantum wells with low defect densities (less than 10,000 defects per square cm) on both polar and non-polar Gallium Nitride substrates. *FY 2010 Plans:* - Demonstrate room temperature pulsed laser diodes at 500 nm with 200 milliwatts output laser power. - Demonstrate operation of a laser diode with differential efficiency of twenty percent. - Demonstrate stable operation of a VIGIL laser for 500 hours.	6.588	5.832	5.848	
Quantum Sensors	0.000	9.000	10.000	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
(U) The Quantum Sensors program is developing approaches to exploit non-classical effects called entanglement to improve the resolution and range of military sensors. The objective of the program is to enhance sensitivity, resolution, and effectiveness of electromagnetic sensors beyond what is classically possible. The theoretical proof stage of the Quantum Sensors program was funded in FY 2007 and 2008 under PE 0601101E, Project MS-01. In that stage, sensors that propagate entangled light out to and back from a target (Type I) were proven to be ineffective when realistic scattering and absorption occur between the source and the target. Sensors that propagate classical light to the target but use entangled light only in the receiver (Type II) were shown to provide qualitative advantages over their classical counterparts. These include compensation for soft aperture losses using squeezed vacuum injection and compensation for detectors' quantum inefficiency using noiseless amplification. A new approach that retains entangled light in the receiver and transmits it to the target (Type III) was discovered and promises substantial enhancements over detection and imaging of targets in the presence of high levels of noise and loss. *FY 2009 Plans:* - Begin engineering of sensor systems based on entangled light. - Demonstrate and quantify compensation of soft aperture loss by squeezed vacuum injection in homodyne laser radar in a range environment. - Demonstrate noiseless amplification for sensors with low quantum efficiency. - Design a quantum illumination system prototype. *FY 2010 Plans:* - Build and field test prototype entangled laser radar. - Demonstrate detection using quantum illumination in laboratory and range environments.				
Parametric Optical Processes and Systems (POPS) (U) The Parametric Optical Processes and Systems (POPS) program will demonstrate all optical signal processing based on Four Wave Mixing (FWM) in optical fibers and using silicon waveguides to achieve data rates of 100 Gigabits per second (Gb/s) to 1 Terabit per second (Tb/s). This program will develop components such as wavelength-shifting wideband amplifiers, tunable optical delays, and parametric sampling for this application. These components will be used in higher level sub-systems such as	1.145	2.142	3.877	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
serializers, de-serializers, and wavelength grooming devices at high data rates of 100 Gb/s - 1Tb/s. These demonstrations of functionality will also include quantitative bit error rate measurements. POPS components and subsystems will enable optical communications at data rates ten times higher than currently possible with conventional approaches. POPS technology will allow all optical manipulation of high rate data streams with a precision and flexibility not currently possible. *FY 2008 Accomplishments:* - Demonstrated enhanced non-linearities of silica fibers and silicon waveguides. - Demonstrated two-pump method for generation of 160 Gigabit per second (Gb/s) Data Streams. - Demonstrated 403 nanosecond (ns) tunable optical delay elements. *FY 2009 Plans:* - Demonstrate serializer component with data rate of 320 Gb/s. - Demonstrate deserializer component with granularity of 40 Gb/s. - Demonstrate 500 ns continuous parametric delay technology. *FY 2010 Plans:* - Demonstrate enhanced serializer component with data rate of 640 Gb/s. - Demonstrate enhanced deserializer component with granularity of 10 Gb/s. - Demonstrate 3000 ns continuous parametric delay technology.				
Spin Torque Transfer-Random Access Memory (STT-RAM)*	9.310	2.818	8.167	
*Formerly titled Miniature, Room Temperature, Ultra-sensitive Magnetic Sensor (MRUMS). (U) The Spin Torque Transfer-Random Access Memory (STT-RAM) program (reclassified from PE 0603739E, Project MT-15) will develop materials and processes to fully exploit the spin-torque transfer (STT) phenomenon for creating “universal” memory elements. This program will develop the core technology for exploiting spin-torque transfer and related phenomena for producing large-scale memories. Compatibility and stability with expected mainstream processes for semiconductor electronics				

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
and patterned media is an important attribute that should enable significant leverage for these new technologies in delivering early demonstrations and in gaining wider acceptance. *FY 2008 Accomplishments:* - Developed magnetic materials that allow for fast, low power switching in the Spin Torque Transfer (STT) architecture. *FY 2009 Plans:* - Develop fabrication techniques and device architectures that exploit the materials. *FY 2010 Plans:* - Develop magnetic materials and architectures that allow for fast low power switching in a STT architecture. - Demonstrate fast low power STT memory cell that has size and endurance similar to current non-volatile electronic memories.					
Design Tools for 3-Dimensional Electronic Circuit Integration (U) The Design Tools for 3-Dimensional Electronic Circuit Integration program developed a new generation of Computer Aided Design (CAD) tools to enable the design of integrated 3-Dimensional (3-D) electronic circuits. The program focused on methodologies to analyze and assess coupled electrical and thermal performance of electronic circuits and tools for the coupled optimization of parameters such as integration density, cross talk, interconnect latency and thermal management. The goals of this initiative were to develop a robust 3-D circuit technology through the development of advanced process capabilities and the design tools needed to fully exploit a true 3-D technology for producing high performance circuits. The deliverables from this program will have a significant impact on the design of mixed signal (digital/analog/ radio frequency) systems and Systems-on-a-Chip for high performance sensing, communications, and processing systems for future military requirements. *FY 2008 Accomplishments:* - Completed 3-D process technology development.		7.442	0.000	0.000	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
- Developed several compelling applications to map into the 3-D technologies. - Completed fabrication of 3-D demo design chips.				
Self-HEALing mixed-signal Integrated Circuits (HEALICs) (U) The goal of the Self-HEALing mixed-signal Integrated Circuits (HEALICs) program is to develop technologies to autonomously maximize the number of fully operational mixed-signal systems-on-a-chip (SoC) per wafer that meet all performance goals in the presence of extreme process technology variations, environmental conditions, and aging. This program is an outgrowth of mixed signal development in the Design Tools for 3-Dimensional Integrated Circuit program. Virtually all DoD systems employ mixed-signal circuits for functions such as communications, radar, navigation, sensing, high-speed image and video processing. A self-healing integrated circuit is defined as a design that is able to sense undesired circuit/ system behaviors and correct them automatically. The motivation for this program came from findings under the TRUST program that, as semiconductor process technologies are being scaled to even smaller transistor dimensions, there is an exponential increase in intra-wafer and inter-die process variations, which have a direct impact on realized circuit performance manifested as significantly reduced yields of fabricated fully operational SoC. The core goal of the HEALICs program is to regain this lost performance. Additionally, the technology developed under this program is expected to address environmental variations and aging as well. Consequently, the long-term reliability of DoD electronic systems is expected to be significantly enhanced. *FY 2009 Plans:* - Develop self-healing control for individual sub-blocks within a larger mixed-signal core. - Integrate sub-blocks into larger mixed-signal cores (anticipated transistor counts in the 1k-10k range). - Develop global self-healing control algorithms. *FY 2010 Plans:* - Continue development of self-healing mixed-signal cores. - Demonstrate increase in performance yield of mixed-signal cores to greater than seventy-five percent with minimal power and die area overhead.	0.000	11.500	13.590	
COmpact Power Processing Electronics Research (COPPER)	0.000	0.000	7.000	

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B. Accomplishments/Planned Program ($ in Millions)		**FY 2008**	**FY 2009**	**FY 2010**	**FY 2011**
(U) The COmpact Power Processing Electronics Research (COPPER) program will address the fundamental limitations of power conversion by enabling a new technology and approach that exploits advances in basic power devices that can operate at very high frequencies with low losses. A key benefit of these new devices is that they can be integrated into very compact circuits and assemblies that will provide dramatic advances to the power bus of a platform. Specifically, this program will develop the technology to enable DC to DC power conversion for military applications at the scale of an integrated circuit so it can be embedded within the electronics subsystem and a new distributed power architecture can be realized. The focus of this program is on attaining 100MHz internal operation frequencies of power circuits since the size of the passive elements (inductors and capacitors) in a power converter scales as the fourth power of the internal operating frequency. *FY 2010 Plans:* - Complete design and initial fabrication of critical sub-circuits and perform measurements in laboratory. - Complete theoretical design and analyses for understanding of the high-frequency trade-off space of relevant circuit designs and topologies.					
Highly Linear Ultra-low Power RF-FETs using CNTs (ULP-LINFET) (U) The objective of the Highly Linear Ultra-low Power RF-FETs using CNTs (ULP-LINFET) program is to develop radio frequency (RF) field effect transistors (FET) using a layer of 1-Dimensional (1-D) aligned carbon nanotubes (CNTs) as the conduction channel to achieve high linearity and ultra-low power for defense sensor systems. CNTs, due to their one-dimensional physics and high current carrying capacity, offer the unique opportunity to achieve highly-linear, high-frequency, and ultra-low power in FET devices. Linearity of RF devices is extremely important in signal rich environments such as noisy battlefields with extensive jamming. Highly linear low noise amplifiers are critical for applications such as: RF front-end processing, broad-band digital communication, radar, synthetic aperture radar (SAR), electronic and signal intelligence (ELINT, SIGINT), electronic sensing (ESM), electronic warfare (EW) and other sensor systems employed in surveillance and reconnaissance C4ISR systems. *FY 2010 Plans:* - Develop techniques for fabricating large/dense 1-D arrays of parallel aligned CNTs.		0.000	0.000	5.187	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
- Develop method for the elimination of metallic CNTs without disruption of the remaining semiconducting CNTs by selective laser ablation or electro-plating. - Demonstrate ultra-low power low-noise amplifier while maintaining high linearity. - Demonstrate RF performance with maximum frequency of greater than 50 Gigahertz (GHz).				
Millimeter-wave All-Silicon Transmitters (MASTR) (U) The goal of the Millimeter-wave All-Silicon Transmitter (MASTR) program is the development of revolutionary high-power/high-efficiency/high-linearity single-chip millimeter (mm)-wave transmitter integrated circuits (ICs) in leading edge silicon technologies. The high levels of integration possible in silicon technologies enable on-chip linearization, complex waveform synthesis, and digital calibration and correction. Military applications include ultra-miniaturized transceivers for satellite communications-on-the-move, collision avoidance radars for micro-/nano-air vehicles, and ultra-miniature seekers for self-guided munitions. The technology developed under this program could also be leveraged to improve the performance of high-power amplifiers based-on other non-silicon technologies through heterogeneous integration strategies. Significant technical obstacles to be overcome include the development of efficient circuits for increasing achievable output power of silicon devices (e.g., effective breakdown voltage enhancement, power combining) at mm-waves; scaling high-efficiency amplifier classes to the mm-wave regime; robust mixed-signal isolation strategies; and thermal management considerations. *FY 2010 Plans:* - Demonstrate high-power (Watt-level), high power-added-efficiency (greater than or equal to fifty percent) power amplifier (PA) circuits at Q-band frequencies. - Develop design techniques for on-chip linearization of high-efficiency silicon PAs.	0.000	0.000	4.000	
Transmit and Receive Optimized Photonics (TROPHY) (U) The objective of the Transmit and Receive Optimized Photonics (TROPHY) program is to develop ultra-wideband (0.1 to 20 Gigahertz (GHz)) photonic components (Photodetectors & Modulators) with significantly enhanced efficiency in comparison to conventional electronics for applications in antenna Transmit/Receive modules. It is expected that such components would have a significant impact on wideband, multi-functional, multi-beam, Active Electronically Steerable Array (AESA) antennas.	0.000	0.000	5.500	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
Furthermore TROPHY components will obviate several thousands of co-axial cables per array replacing these with a much lighter and significantly broader band optical fiber. By developing modulators and detectors independently optimized for transmit and receive applications, TROPHY will deliver application specific, best in class components. *FY 2010 Plans:* - Enhance third-order intercept point (OIP3) of the Transmit link to +65 decibels relative to a milliwatt of power (dBm). - Enhance gain of the Receive link to 35 dB.				
Nitride Electronic NeXt-Generation Technology (NEXT) (U) The NEXT program will develop innovations in the area of advanced nitride electronics. Research will focus on innovative approaches to enable revolutionary advances in nitride electronic devices and integrated circuits resulting in the ability to operate at very high frequencies while maintaining extremely favorable voltage breakdown characteristics. *FY 2010 Plans:* - Develop self-aligned structure with short gate length, novel barrier layers and reduced parasitics. - Develop transistor models.	0.000	0.000	4.500	
3-D Technology for Advance Sensor Systems (U) The 3-D Technology for Advance Sensor Systems effort exploited 3-Dimensional (3-D) technology for applications in Advance Sensor Systems. *FY 2008 Accomplishments:* - Applied 3-D technology to device implementation. *FY 2009 Plans:* - Continue 3-D device development.	2.400	1.440	0.000	
Indium Based Nitride Technology Development	0.000	3.000	0.000	

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B. Accomplishments/Planned Program ($ in Millions)	FY 2008	FY 2009	FY 2010	FY 2011
FY 2009 Plans: - Initiate Indium Nitride development.				
Secure Media and ID Card Development *FY 2009 Plans:* - Initiate ID card development.	0.000	0.240	0.000	

C. Other Program Funding Summary ($ in Millions)

N/A

D. Acquisition Strategy

N/A

E. Performance Metrics

Specific programmatic performance metrics are listed above in the program accomplishments and plans section.